IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SANDISK CORPORATION, No. C-01-4063 VRW

Plaintiff, ORDER

v

MEMOREX PRODUCTS, INC, et al,

Defendants.

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This action involves a patent dispute between SanDisk, the patent holder, and various companies that allegedly infringe SanDisk's patent. SanDisk and defendant Ritek filed a joint claim construction statement on August 2, 2002. Doc # 116. Defendants Memorex and Pretec joined in this claim construction statement February 19, 2003. Doc # 242. Ritek moves the court for summary judgment of non-infringement based on this claim construction. Doc # 208. Defendants Memorex and Pretec attempt to join in Ritek's summary judgment motion. See Doc # 236. Based on the analysis below, the court DENIES the Memorex and Pretec notice of joinder in Ritek's motion for summary judgment.

Based on the court's construction of the relevant claim terms, the court GRANTS Ritek's motion for summary judgment.

I

The court must consider two preliminary matters before reaching claim construction and Ritek's summary judgment motion. First, the court considers Ritek's miscellaneous administrative request to strike SanDisk's claim construction statement of February 20, 2003. Doc # 245. Memorex and Pretec were previously represented by Thomas Jeing. Due to Mr Jeing's improper conduct, Memorex and Pretec failed to participate with SanDisk and Ritek in the August 2, 2002, claim construction statement. Doc # 225. On January 16, 2003, the court held a case management conference (CMC) with the parties. At the CMC, Memorex and Pretec were given leave to raise new claims construction issues in a schedule adopted by the court. The court also added the following limitation:

> If no new issues are raised in the Memorex and Pretec Invalidity Contentions or Proposed Construction Statement, no additional briefing will be permitted.

Minute Order (Doc # 240) at 1.

SanDisk and defendants Ritek, Memorex and Pretec understood the court's direction differently. The parties all understood the order to forbid further claim construction briefs if Memorex and Pretec raised no new issues. The parties differed in their understanding whether the order required an updated claim construction brief if no new issues were raised. SanDisk understood the order to require an updated joint claim construction statement including all defendants without regard

to whether Memorex and Pretec raised any new issues. Defendants understood the order to forbid filing an updated joint claim construction statement unless Memorex and Pretec raised new issues.

Memorex and Pretec did not raise any new claim construction issues. Doc # 242 (adopting the previous claim construction). According to its understanding, SanDisk attempted to meet-and-confer with defendants to produce an updated claim construction statement. Upon defendants' refusal to cooperate, SanDisk filed a claim construction statement. Doc # 244. This statement contains minor alterations from the August 2, 2002, statement. According to defendants' understanding, they refused to take part in filing an updated claim construction statement. See Docs ## 244, 245. Defendants now request the court to strike SanDisk's updated claim construction brief of February 20, 2003. Defs Admin Request (Doc # 245).

The court finds that it was not improper for SanDisk to act on its understanding of the court's order. Accordingly, the court DENIES defendants' motion to strike the February 20, 2003, claim construction statement. The court notes, however, that the differences between the February 20, 2003, statement and the August 2, 2002, statement are insignificant and accordingly chooses to rely exclusively on the earlier August 2, 2002, statement and the accompanying briefs.

Second, the court considers the Memorex and Pretec notice to join in Ritek's motion for summary judgment. Doc # 236. Neither Memorex nor Pretec has presented any facts

related to the functioning of their accused devices. In order for the court to decide a motion for summary judgment, it must have facts related to each individual defendant before it. Accordingly, the court DENIES Memorex and Pretec's attempt to join Ritek's summary judgment motion. If Memorex and Pretec seek to move for summary judgment, they must do so by filing a duly noticed motion accompanied by affidavits that describe their individual products. See Civ LR 56-1.

II

A

SanDisk designs and manufactures CompactFlash memory cards. CompactFlash cards are memory storage units used in many electronic devices, including personal digital assistants, digital cameras and MP3 players. SanDisk owns United States Patent No 5,602,987 ('987 patent). The '987 patent covers a method of using electrically erasable programmable read only memories ("EEprom"). '987 patent at 1. EEprom memory is different from conventional hard drive memory because EEprom memory is solid state, which means that EEprom memory does not have any moving mechanical parts. EEprom memory is similar to conventional hard drive memory in that it is non-volatile, which means that its memory can be maintained without a continuous power source. Some of the advances over the prior art described in this patent include the ability to select sectors of memory individually and in groups, erase such a group of sectors simultaneously, perform read/write functions on sectors

simultaneously with erase functions on other sectors and map defective memory cells at the sector level. Id at 1:60-2:63.

Claims 1 and 10 are two of the '987 patent's five independent claims and contain the only terms that are disputed by the parties. See Docs ## 136, 148. Claims 1 and 10 describe a method of operating a computer system that includes a processor and a memory system. The memory system contains a memory controller and an EEprom array. '987 patent at Fig 1a.

The EEprom array is an array of non-volatile floating gate memory cells. The EEprom array is subdivided into sectors, which each contain at least a user data portion and an overhead portion. Id at 8:40-51. The user data portion contains the information the user has designated to be stored. User data includes, for example, music files, digital images and text documents. The overhead portion contains information used to regulate the memory system. Overhead data may include, for example, identifying information about the sector and information used to detect and manage defects. The relative proportion between the user data portion and the overhead portion can be changed over time. Id at 8:59-67. Additionally, the user data and overhead portions do not need to be grouped together physically. Id.

When erasing data from the array, the controller relays command and address information to the EEprom array. The commands are "gated by the address decode," so that the command "is effective only on the sector that is being addressed." Id at 5:46-55. This gating function allows the sectors to be erased simultaneously. It also results in less "over-erasing,"

because individual sectors can be examined during the process of erasing to verify that the command given to that sector has been executed. For example, if an erase command is given to a large number of sectors, some sectors will finish erasing earlier than others. These sections can be de-selected for any subsequent erase commands initiated to complete the original erase command.

When reading or writing to the memory sectors, the controller interacts with the information contained in the memory sector. The controller shifts out the address and read or write command information to the EEprom array, which sends the command to the appropriate memory sector and returns data from the memory sector through a variety of components. The controller then relays the data to the processor.

The use of overhead data allows the memory system to identify and correct for defects on a more efficient and dynamic basis. '987 patent at 7:31-8:39. Memory defects may be either hard or soft. Hard defects are physical defects in the memory medium. Soft defects are temporary defects in a particular read, write or erase command. Because EEprom memory degrades more quickly than traditional disk drives, compensating for hard defects in an efficient manner is more important. To compensate for hard defects, the patent method includes defect-related information in the overhead portion of the memory sectors. This information allows the memory system to manage defects at the memory cell level, rather than merely at the sector level. Such defect management can occur on a dynamic basis.

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Ritek also manufactures memory cards. Ritek's cards share many characteristics with SanDisk's cards. The cards contain a controller and an EEprom array. Chiu Decl (Doc # 284, Exh K) ("Chiu Decl I") at ¶ 2. Ritek's EEprom array is subdivided into blocks, which are the basic unit of erase for the Ritek cards. Id at ¶ 3. Accordingly, for purposes of this order, "blocks" in Ritek's products correlate to "sectors" in the '987 patent. A typical Ritek block contains both a user data portion and an overhead portion.

Not all Ritek's blocks, however, are typical. Ritek's cards contain some blocks that consist of only overhead data. The nature and number of these overhead-only blocks depends on the particular controller used in the Ritek card. Ritek cards that use an SSS controller contain three types of overhead-only blocks. Chiu Decl I (Doc # 284, Exh K) at ¶ 4. First, "Windows Information Blocks" store a variety of overhead data, including a "map between logical addresses and physical locations within the memory, flags indicating bad blocks, error correction codes, and information about blocks containing data." Id at ¶ 7. Second, "Spare Pointer Blocks" also store only overhead data. Spare Pointer Blocks are used in defect management to store data that indicate which blocks are defective and which blocks are to be used as spare blocks. Id at ¶ 6. Third, Ritek's cards utilize "Boot Blocks" that contain the information necessary to begin accessing the memory array. Id at ¶ 5.

Ritek cards that use a KTC controller contain two types of overhead-only blocks. Chiu Decl (Doc # 284, Exh J) ("Chiu

Decl II") at ¶ 3. First, "Defect Management Table Blocks" are used to store only overhead information relating to "blocks that are originally marked as defective by the manufacturer of the memory array." Id at ¶ 4. Second, "Spare Management Table Blocks" are used to "store information about which block is currently storing overwrite data in the Spare Block." Id at ¶ 5.

The court will collectively refer to these as the overhead-only blocks, because the overhead-only blocks in Ritek cards that contain SSS controllers are not materially different, for present purposes, from the overhead-only blocks in the cards that contain KTC controllers. Without these overhead-only blocks, Ritek's memory cards would not operate. Chiu Decl I (Doc # 284, Exh K) at ¶ 8; Chiu Decl II (Doc # 284, Exh J) at ¶ 6.

III

Infringement analysis is a two-step process, beginning with a determination of the "meaning and scope of the patent claims," and ending with a comparison of the "properly construed claims to the device accused of infringing." Markman v Westview Instruments, Inc, 52 F3d 967, 976 (Fed Cir 1995). Determining the meaning and scope of the claims is a question of law and may be decided in a claim construction order. Id.

When evaluating the meaning and scope of the claims, the court considers the intrinsic evidence, first looking to the patent claims, then to the specification and finally to the prosecution history. Vitronics Corp v Conceptronic, Inc, 90 F3d

1576, 1582-83 (Fed Cir 1996). Unless "compelled otherwise," the court is bound to give a claim term the "full range of its ordinary meaning as understood by persons skilled in the relevant art." Texas Digital Systems, Inc v Telegenix, Inc, 308 F3d 1193 (Fed Cir 2002); York Prods, Inc v Central Tractor Farm & Family Ctr, 99 F3d 1568, 1572 (Fed Cir 1996). A court may limit the scope of the claim term in any of the following four situations:

> First, the claim term will not receive its ordinary meaning if the patentee * * * clearly set forth a definition of the disputed claim term in either the specification or prosecution history. Second, a claim term will not carry its ordinary meaning if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention.
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> Third, * * * a claim term also will not have its ordinary meaning if the term chosen by the patentee so deprives the claim of clarity as to require resort to the other intrinsic evidence for a definite meaning. Last, as a matter of statutory authority, a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto, if the patentee phrased the claim in step- or means-plus- function format.

CSC Fitness, Inc v Brunswick Corp, 288 F3d 1359, 1366-67 (Fed Cir 2002).

After considering the claims, the court should look to the specification. It is "always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning." Vitronics, 90 F3d at 1582. In fact, review of the specification is "the single best guide to the meaning of a disputed term." Id. A court, however, is not allowed to read limitations into

the claims from the specification. Teleflex, Inc v Ficosa North America Corp, 299 F3d 1313 (Fed Cir 2002).

The final intrinsic evidence available to the court is the prosecution history, which may estop the patentee from claiming an expansive definition. Where the patentee has disclaimed an interpretation of the claims in the course of obtaining the patent, the court must exclude the disclaimed interpretation. Southwall Tech, Inc v Cardinal IG Co, 54 F3d 1570, 1576 (Fed Cir 1995). If the disclaimer occurred through an argument, rather than an amendment, the disclaimer must be "clear and unmistakable." Omega Engr, Inc v Raytek Corp, 334 F3d 1314, 1325-26 (Fed Cir 2003). A disclaimer is not clear and unmistakable if the disclaimer is amenable to "multiple reasonable interpretations." Id at 1324 (finding that prosecution disclaimer is not clear and unmistakable if the disclaimer is "too vague or ambiguous").

In most cases, the court will be able to resolve all claim construction issues based on the intrinsic evidence. Only where necessary should the court resort to extrinsic evidence. Vitronics, 90 F3d at 1583. In this case, the intrinsic evidence is sufficient to decide the case. Accordingly, the court does not rely on the extrinsic evidence in construing the patent claims at issue.

## IV

In March 1998, SanDisk brought a patent infringement action against Lexar Media, Inc ("Lexar") under the '987 patent. The case was decided by the Honorable Charles R Breyer who

issued a claims construction order following a hearing and briefing. See SanDisk Corp v Lexar Media, Inc, 1999 WL 129512 (ND Cal) (Lexar (claim construction)). Both SanDisk and Ritek agree that the court should rely on Judge Breyer's claim construction. The parties disagree, however, about the extent to which the Lexar claim construction covers terms at issue in this suit. The court hereby adopts the following relevant definitions from Judge Breyer's claim construction order based on the reasonableness of the constructions.

> A "non-volatile memory sector" is the basic unit of erase for the non-volatile memory. It is not limited to 512 bytes of user data and 64 bytes of overhead data.
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> * * *
>
> "Partitioned" refers to either logically dividing or physically dividing the memory into a plurality of sectors. When the patent refers to the memory array being "partitioned" into sectors it is not necessarily referring to the physical division of the memory into sectors such that each sector must be physically separated from the adjoining sectors.

Id at *2-*3.

V

Ritek moves for summary judgment on one basis only. Ritek Br (Doc # 208) at 2.

> Ritek is entitled to summary judgment of non-infringement of SanDisk's '987 patent because all of Ritek's accused products lack a critical requirement of the claims. SanDisk's asserted claims all require that each sector of memory cells have both a user data and overhead portions. But it is undisputed that Ritek's

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> accused products have blocks that do not have any user data portion.

Id. Due to the limited nature of Ritek's summary judgment motion, the court need only construe two disputed claim terms to determine whether summary judgment should be granted.

A

"Array of non-volatile floating gate memory cells" (Claims 1 & 10)

Construction: An array of non-volatile floating gate memory cells contains a group of memory cells on one or more memory chips. Multiple chips in the same array are connected through objects such as a common interface and/or common logic and resistor circuits. An array may contain components that are not memory cells, such as an interface.

The parties dispute whether the term "array" includes memory cells from a single chip only or from any number of chips. SanDisk Br (Doc # 136) at 9-11; Ritek Br (Doc # 148) at 13. The specification uses the term "array" in two ways. First, the specification describes an array of memory cells contained on a single memory chip (an intra-chip array). '987 patent at 1:65-67 (describing an "array of Flash EEPROM cells on a chip") (emphasis added); see id at 5:5-21 (describing the partitioning of memory cells contained on a chip into sectors). Second, the specification also describes an array of memory cells contained on one or more memory chips (an inter-chip

array). Id at 3:61 (specifying "an array 33 of EEPROM circuit chips) (second emphasis added); id at 13:60-63 ("[T]he Flash EEPROM memory array 33 is organized into sectors * * * such that all memory cells within each sector are erasable together."); Fig 1B (including multiple chips within the memory array 33).

The parties each note one of the two uses of the term "array" in the specification and ignore the other. SanDisk Br (Doc # 136) at 9-11; Ritek Br (Doc # 148) at 13. SanDisk asserts that the intra-chip interpretation should be adopted, whereas Ritek asserts that the inter-chip interpretation should be adopted. The court must determine which of the two interpretations of "array" used in the specification is intended in claims 1 and 10. The text of the claim header for each claim describes:

> an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit.

'987 patent at 16:26-29 (Claim 1); id at 17:32-35 (Claim 2). This section of the claims, by itself, provides little guidance because it gives no indication whether the array of memory cells must be contained on only one memory chip or whether the array may extend to more than one chip.

Comparing the claim header with the specification suggests that the claim describes an inter-chip array. The claim header is quoted above in the previous paragraph. The specification states:

> [T]he Flash EEPROM memory array 33 is organized into sectors * * * such that all memory cells within each sector are erasable together.

Id at 13:60-63. The language from the claims and the specification is virtually identical, which suggests that the "memory array 33" is the memory array described in the claims. The "Flash EEPROM memory array 33" is described earlier in the specification as "an array 33 of EEPROM integrated circuit chips." Id at 3:61 (emphasis added). Accordingly, this suggests that the "array" in claims 1 and 10 is an inter-chip array.

The minor textual differences between the two passages do not change this interpretation. First, the claims describe an array "partitioned into a plurality of sectors," id at 16:26-29, whereas the specification describes an array "organized into sectors," id at 13:60-63. In this context, the words "partitioned" and "organized" have identical meanings and the insertion of the phrase "into a plurality of" is mere surplusage. Second, the claims describe the sectors as "individually includ[ing] a distinct group of said array of memory cells that are erasable together," id at 16:26-29, whereas the specification describes a sector as an object "such that all memory cells within each sector are erasable together," id at 13:60-63. The only difference is the inclusion of the phrase "individually includ[ing] a distinct group," which is mere surplusage. Both the claims and the specification describe a sector as the "basic unit of erase." See Lexar (claims construction), 1999 WL 129512 at *2-3.

The use of the term "array" in the elements of the claims also suggests that an inter-chip array is described. The first element of both claims 1 and 10 reads "providing said

memory array and a memory controller within a card." Id at 16:30-32, 17:36-38. The word "said" indicates that the array described in the element is the same as in the header. The important aspect from the text of the element is that the element connects together the array and the controller. This connection is repeated frequently throughout the specification. Figures 1A, 1B, 2, 6 and 7, as well as the text of the specification accompanying those figures, connect together the controller and the array. In each instance, the array described is the memory array 33. See, e g, id at Fig 1A. As noted above, the memory array 33 is an inter-chip array.

An intra-chip array is never described in any of the figures. Figures 1B and 2 provide opportunities for such an array to be described, because individual chips are displayed. In neither figure, however, is an individual chip described as an array. To the contrary, the term "array" is used to describe a set of one or more chips. See, e g, id at 4:1, 7-8 ("Referring to FIG 1B, * * * [t]he EEPROM array 33 includes a number of integrated circuit chips 43, 45, 47, etc.").

Accordingly, the court finds that an inter-chip array is described in claims 1 and 10. It should be noted that the memory system may contain more than one memory array. "For large amounts of memory, that which is conveniently provided by a single array 33 may not be enough. In such a case, additional EEPROM arrays can be connected * * * ." Id at 4:26-30. Figure 1B carefully delimits an array using a box. Inside the box are one or more memory chips that are connected to a common interface and common logic and resistor circuits. The court,

therefore, finds that the memory chips linked to common objects, such as a common interface and/or common logic and resistor circuits constitute the memory chips contained in a single array. Finally, the court notes that the array is described as an array of memory cells, but figure 1B includes items, such as the interface, which are not memory chips. Accordingly, the court also finds that the array is not limited to memory chips.

B

"[P]artitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion." (Claims 1 and 10)

Construction: Each non-volatile memory sector contained within an array of non-volatile floating gate memory cells must include at least one user data portion and one overhead portion. Memory sectors are not limited to only one user data portion and one overhead portion.

SanDisk makes a variety of arguments to prove that claims 1 and 10 require only some of the non-volatile memory sectors to be partitioned into at least user data and overhead portions. Before considering the intrinsic evidence presented in this motion, the court notes that this claim has been previously construed in the Lexar litigation as well as by the court previously in its order denying SanDisk's motion for a preliminary injunction. In Lexar, Judge Breyer found that the

term "user data and overhead data portions" should be construed in the following manner:

> Each non-volatile memory sector must have at least one user data portion and one overhead data portion, but is not limited to only one data user [sic] portion and only one overhead data portion.

Lexar (claim construction), 1999 WL 129512 at *3. SanDisk argues that this construction should be interpreted to require only those memory sectors that contain user data to also contain overhead data. SanDisk's argument draws some strength from the limited nature of the Lexar court's construction. The Lexar court did not explicitly construe the broader phrase from the patent, "partitioning the memory cells within the individual sectors into at least a user data portion and an overhead data portion." The Lexar court limited its construction to the "user data and overhead data portions" of claims 1 and 10. Id at *2-3.

Still, SanDisk's argument ultimately fails because the Lexar construction implicitly suggests that it was construing the broader phrase in that the construction includes the requirement that "[e]ach non-volatile memory sector" must be partitioned into both user data and overhead portions. Id. The court finds that the Lexar court intended to construe the broader term, including each non-volatile memory sector, rather than merely those that already contain user data. This construction comports with the court's independent analysis of the proper construction of the claims of the '987 patent.

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SanDisk argues that requiring each sector to contain both user data and overhead portions conflicts with the language of the patent claims in two ways. SanDisk Br (Doc # 136) at 15. The patent claim is written using the term of art "comprising." Id at 16. A claim containing the term "comprising" signals that "additional steps may be performed in carrying out [the] claimed method." Smith & Nephew, Inc v Ethicon, Inc, 276 F3d 1304, 1311 (Fed Cir 2002). SanDisk argues that the use of the word comprising means that the memory system may contain sectors composed of only overhead data. SanDisk's argument fails because the parties do not dispute an additional step. The parties dispute the proper interpretation of the partitioning step, which is required by the claim as written.

Second, SanDisk claims that "there is no language in claim 1 such as 'all,' 'every' or 'without exception' that would support the limitation that Ritek seeks to read into the claim." SanDisk Br (Doc # 136) at 15. The court finds to the contrary based on the use of the word "the" in the claim. The claim term in question describes "partitioning the memory cells within the individual sectors." '987 patent at 17:42-44 (emphasis added). The cells and the sectors described in the disputed claim term refer to the cells and the sectors described in the claim header. See, e g, id at 17:32-35 (referring to "a memory system [that] includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit."). By using the definite article

"the," the claims require that each of the sectors contained in the array of non-volatile floating gate memory cells be partitioned. The claims also require that all of the memory cells within the individual sectors be partitioned in such a way to include at least a user data portion and an overhead portion. If the claim term in dispute were written differently, a different result would obtain. SanDisk's interpretation would be controlling if the claim term were written "partitioning memory cells within individual sectors" or if it were written "partitioning some of the memory cells within some of the individual sectors." Accordingly, the court rejects SanDisk's attempt to construe, based on the patent text, the partitioning requirement to apply to only some of the sectors contained within the memory array.

SanDisk also argues that the structure and function of the method claim demonstrates that only some of the sectors must be partitioned. SanDisk states, "This step in claim 1 refers to dividing (logically or physically) the individual non-volatile memory sectors used by the memory system of the computer system in the practice of method claim 1 into at least one user data portion and at least one overhead data portion." SanDisk Br (Doc # 136) at 15 (emphasis added). The court agrees with Ritek, which argues that SanDisk's proposed construction is redundant at best. Ritek Br (Doc # 148) at 21 ("If the step is recited in the claim, then it is already part of the claimed method."). The court rejects SanDisk's attempt to narrow the function of method claims 1 and 10 to merely the storage of user data with overhead. Although some steps of claims 1 and 10 are

limited to writing and reading user data to a sector, claims 1 and 10 include other steps that describe other functions, including designating sectors and defect management.

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SanDisk offers a number of examples from the patent specification that allegedly demonstrate embodiments covered by the claims that do not contain both user data and overhead portions. Ritek argues that figure 5 represents the only embodiment of a sector in the patent. Ritek Br (Doc # 148) at 17. Ritek's argument fails because the patent itself describes figure 5 as merely a "typical sector," not the only embodiment of the sector. '987 patent at 8:44.

First, SanDisk offers empty sectors, i e, sectors in an erased state, as examples of sectors that do not contain both user data and overhead data. SanDisk Br (Doc # 136) at 18-19 ("Non-volatile memory sectors in an 'erased' state do not store both user data and overhead data."). The court rejects this reasoning, because the method requires only that the sectors be partitioned into portions; the method does not require that the portions actually store data. Additionally, SanDisk has argued that only those sectors used in the practice of the method should be considered. To the extent that a sector remains unused, it is difficult to argue that the sector is used in the practice of the method.

Second, SanDisk claims that defective sectors store only overhead data. SanDisk Br (Doc # 136) at 16-17 ("Because such sectors will not store user data, the sectors * * * will

not be partitioned into the user data and overhead regions."). As mentioned above, the method only requires partitioning, not actual storage of data. The mere fact that a sector will not contain user data does not mean that it does not have a user data portion. An unusable user data portion is still a user data portion.

Third, SanDisk argues that the sector defect map described in the specification contains only overhead data. SanDisk Br (Doc # 136) at 17-18. A whole sector may be marked as defective if a sufficiently large number of cells within a sector becomes defective. In such a situation, no additional user data are stored in that section and the controller uses a defect pointer to write data to a different sector. The patent specification states:

> The defect pointer for the linked sectors may be stored in a sector defect map. The sector defect map may be located in the original defective sector if its spare area is sufficiently defect-free. However, when the data area oft he [sic] sector has accumulated a large number of defects, it is quite likely that the spare area will also be full of defects.
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> Thus, it is preferable in another embodiment to locate the sector map in another memory maintained by the controller. The memory may be located in the controller hardware or be part of the Flash EEPROM memory.

'987 Patent at 11:59-12:1.

The fact that the sector defect map contains only overhead data does not prove that the embodiment contemplates sectors with only overhead data. Although the sector defect map is composed entirely of overhead data, the court finds that the sector defect map is located entirely within the overhead portion of a single sector. The term "sector defect map" is

ambiguous and must be read in context. It could refer to either a map that details which sectors are defective (global sector defect map) or it could refer to whether a single sector or portion of a sector is defective (single sector defect map). The court adopts the latter interpretation. The patent language refers to the sector defect map potentially being located "in the original defective sector." Coordinating the sector defect map with the single, original sector suggests that the sector defect map refers only to whether a single sector or a portion of a single sector is defective. It would not be efficient to locate a global sector defect map in every original defective sector.

The context of the discussion of the sector defect map also suggests that it is a single sector defect map. The description of "alternative defects data" is followed immediately by a discussion of the sector defect map. See '987 patent at 11:44-12:6. The discussion of the alternative defects data references figure 5, which contains "alternative defects data" and "defect map" in the overhead portion of a single, typical sector. The proximity of the discussion of alternative defects data and the sector data map in the text suggests that "defect map" in figure 5 is the same as the "sector defect map" described in the text and that these are both single sector defect maps.

The specification describes the possibility that the sector defect map may be "part of the Flash EEPROM memory" rather than located in the "original defective sector." A sector is defined by logical reference to specific physical

locations on the memory chip. Accordingly, the memory cells constituting a sector need not be physically contiguous. The context of the discussion of the sector map quoted above suggests that "part" and "original defective sector" refer to the physical location of the cells within the sector, rather than to the logical delimitation of the sector. This is apparent because the patent suggests that a significant number of cells in the same sector may be defective due to physical damage to the chip. See id at 11:59-12:1 ("[W]hen the data area oft he [sic] sector has accumulated a large number of defects, it is quite likely that the spare area will also be full of defects."). The patent, therefore, suggests that it may be advisable to locate the sector defect map on another physical area of the chip, either as part of the controller or as part of the Flash EEPROM memory.

Accordingly, the court rejects SanDisk's argument that the sector defect map constitutes a sector with an overhead-only portion located in another logical part of the array. The sector defect map is located within the overhead portion of a single, defective sector. Thus, SanDisk's argument here merges into its argument related to defective sectors, which the court rejected above.

Fourth, SanDisk points to cache dumping as a claimed embodiment that "may or may not be partitioned into both user data and overhead portions." SanDisk Br (Doc # 136) at 18. The patent describes embodiments of the invention that include a write cache. Data is stored on a temporary basis in the write cache. In the event of a main power outage, a temporary power

source can be used to transfer the data in the write cache to "the reserved space in the Flash EEPROM memory." '987 patent at 13:39. SanDisk concludes from this that the claimed invention may contain "sectors that are used for overhead purposes only." SanDisk Br (Doc # 136) at 18.

Because the cache dumping description in the specification is ambiguous, it does not aid the court in determining whether all sectors contained in the array must be partitioned into at least user data and overhead portions. SanDisk argues that cache dumping suggests that SanDisk's products may contain overhead-only sectors. SanDisk Br (Doc # 136) at 18. The court notes, however, that a cache is used to store user data, not overhead data. Accordingly, a cache dump is more likely to contain only user data, rather than to contain only overhead data. The specification describes the cache memory as being attached to a "reserved space in the Flash EEPROM memory." '987 patent at 13:39. Later, the specification defines the memory more specifically as the "Flash EEPROM memory 33." Id at 13:51-52. Thus, the cache is attached to the array described in claims 1 and 10. It is unclear, however, whether dumping into a reserved space is any different than reading or writing to the regular sectors. Nowhere in the specification does it discuss whether or not during dumping the sectors within the "reserved space" are partitioned as claims 1 and 10 require. Mere ambiguity in the specification is insufficient to overcome the balance of the evidence, including the language of the claims.

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The prosecution history also supports the construction described above. The court previously found that the prosecution history estops SanDisk from arguing that only some sectors must be partitioned into user data and overhead portions. The court reasoned:

> [I]n responding to the examiner's rejection of claim 85 (which issued as claim 10), SanDisk stated:
>
> > The memory cell array is divided into sectors, with the cells within each sector being erasable together as a unit. Stored in each sector is a sectors [sic] worth of user data and some overhead information (a header) about the sector and/or the user data stored in the sector.
>
> Miclean Decl (Doc # 62), Exh C at SDM000176 (emphasis added). Thus, SanDisk specifically limited its claim to include only those devices in which each sector within a memory cell array contains both overhead and user data. SanDisk cannot now argue that only some of the sectors of a memory cell array need to contain user data and overhead data.

Order (Doc # 106) at 9 (alteration in original).

The patent examiner initially rejected the claims that now constitute claims 1 and 10. These claims were rejected in part because prior art described partitioning a memory into sectors and portions within a sector. Prosecution History (Doc # 137, Exh 9) at SDM 003386 ("Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors. * * * Yorimoto teaches partitioning the cells with[in] a sector into portions, each portion is for storing a specific type of information."). In prosecuting the patent, SanDisk responded that the prior art did not require rejection of its claims for two reasons. First, SanDisk argued that none

of the prior art sources used EEPROM memory to emulate a disk drive. Id at SDM 003412-13. Second, SanDisk emphasized the "sectored and partitioned characteristics" of its invention, especially that the "individual sectors * * * store both user data and overhead data." Id at SDM 003413; id at SDM 003409 ("Stored in each sector is a sectors [sic] worth of user data and some overhead information * * * .").

SanDisk argues that the '987 patent was not distinguished on the grounds that each sector is partitioned into user data and overhead portions. SanDisk Br (Doc # 136) at 6. SanDisk quotes the following section from the prosecution history:

> Claim 79 ['987 Patent - Claim 1] defines a flash EEPROM system with an array that is divided into sectors of cells that are erasable together as a unit. * * * It is the use of this type of memory that allows the memory itself to be operated very similarly to that of a disk drive, with individual sectors that store both user data and overhead data (a header for the sector). It is the operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory that is novel and non-obvious.

Prosecution History (Doc # 137, Exh 9) at SDM03412. SanDisk argues that distinguishing its patent on the grounds that it partitions "individual sectors" does not require that all sectors be so partitioned. SanDisk Br (Doc # 136) at 6-7. SanDisk notably ignores the portions of the prosecution history previously quoted by the court above. One quotation specifically states that user data and overhead data is "[s]tored in each sector." Prosecution History (Doc # 137, Exh 9) at SDM 003409. This language is not susceptible to "multiple

reasonable interpretations," but clearly requires each sector to be partitioned. See Omega Engr, 334 F3d at 1324.

Further, SanDisk's reference to "individual sectors" must be read in the context of the claims of the patent. Claims 1 and 10 refer specifically to "individual sectors" in the partitioning element of the claim. '987 Patent at 16:35-37, 17:42-44 ("[P]artitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion.") (emphasis added). As described above, a reading of the text of the term "the individual sectors" leads to the conclusion that the claim demands that each sector be partitioned into user data and overhead portions.

SanDisk also argues that the prosecution history does not evince a clear and unmistakable surrender, because SanDisk used the word "each" only once in the prosecution history and this usage occurred during the summary of the argument, rather than as part of the actual argument. See SanDisk Br (Doc # 271) at 13-14 (citing Schwing GmbH v Putzmeister Aktiengesellschaft, 305 F3d 1318 (Fed Cir 2002)). SanDisk argues that Schwing requires the court to disregard SanDisk's clear language describing partitioning. See SanDisk Br (Doc # 271) at 13-14. The court disagrees. The Schwing court found that an "equivocal" description of the claims in a "general recitation of the claimed elements" was insufficient to constitute prosecution history estoppel. Schwing GmbH, 305 F3d at 1327. As noted above, the statements made by SanDisk in its arguments to the patent examiner were not ambiguous or equivocal. Additionally, the court finds that SanDisk's statement that

"each sector" must be partitioned into overhead data and user portions was a fundamental part of its argument. The mere fact that SanDisk only used the term "each" once does not control. SanDisk's later emphasis on partitioning into sectors and within sectors, as well as its use of the claim term "individual sectors" is sufficient to demonstrate that one basis upon which SanDisk was asserting patentability was partitioning each sector into at least user data and overhead portions.

Accordingly, the court finds that SanDisk clearly and unmistakably disclaimed coverage of systems in which only some of the sectors in the array were partitioned into at least user data and overhead portions. This finding is supported by the claim terms themselves. The court must indulge a "heavy presumption" if it finds that a claim term does not carry its "full ordinary and customary meaning" because the patent holder made disclaiming arguments during the patent prosecution. Omega Engr, 334 F3d at 1323. In this case, however, the court's prosecution history analysis suggests the same result as its textual analysis of the claims. Accordingly, the court's prosecution history finding is consistent with the heavy presumption.

4

Finally, the analysis above is consistent with the court's previous ruling on the matter. Order (Doc # 106). On May 17, 2002, the court construed the phrase to cover "only devices in which each sector within a memory cell array contains both user data and overhead data." Id at 9. The court adopts a

substantially identical construction today. The only difference is that the court tracks the language of the claim more closely by using "within an array of non-volatile floating gate memory cells" instead of merely using "within a memory cell array."

VI

A

Patent infringement is a two-step analysis. First, the claims are construed by the court as a question of law. Bayer AG v Elan Pharmaceutical Research Corp, 212 F3d 1241, 1247 (Fed Cir 2000). The court's construction of the claims is laid out above. Second, the fact-finder compares the construed claims to the accused device. Id. A plaintiff must demonstrate that the accused device infringes one or more claims of the patent either literally or under the doctrine of equivalents. Id. Literal infringement occurs if the accused device practices all elements of the patent claim. Id at 1247-48.

Infringement under the doctrine of equivalents occurs if the accused device practices each step or an equivalent. Network, LLC v Centraal Corp, 242 F3d 1347, 1354 (Fed Cir 2001). Due attention must be given to the role of each of the claimed steps in infringement analysis under the doctrine of equivalents. Warner-Jenkinson Co v Hilton Davis Chem Co, 520 US 17, 39-40 (1997). Determining whether a device infringes under the doctrine of equivalents is a question of fact. Bayer AG, 212 F3d at 1251. Before the court reaches this question of fact, however, it must "first determine whether the scope of the doctrine of equivalents, as applied to the claim limitations * *

* has been narrowed by the legal doctrine of prosecution history estoppel or proscribed by the 'all elements' rule." Lockheed Martin Corp v Space Systems/Loral, Inc, 324 F3d 1308, 1320 (Fed Cir 2003). Prosecution history estoppel and the all-elements rule are questions of law. See id.

"Prosecution history estoppel requires that the claims of a patent be interpreted in light of the proceedings in the PTO during the application process." Festo Corp v Shoketsu Kinzoku Kogyo Kabushiki Co, 535 US 722, 733 (2002). To the extent that the patentee surrenders patent "territory" during prosecution, the patentee is estopped from asserting that the surrendered territory is covered by the patent. See id at 733-34. A patent holder may be estopped by the prosecution history as a result of claim amendments or arguments made to the patent examiner. In this case, Ritek alleges only argument-based prosecution history estoppel. Ritek Reply (Doc # 286) at 13:14-15. "To invoke argument-based estoppel, the prosecution history must evince a clear and unmistakable surrender of subject matter." Eagle Comtronics, Inc v Arrow Communications Labs, Inc, 305 F3d 1303, 1316 (Fed Cir 2002) (internal quotation omitted). Thus, the standard for argument-based estoppel is the same as the standard for prosecution disclaimer, discussed above. See Omega Engr, Inc v Raytek Corp, 334 F3d 1314, 1326 n1 (Fed Cir 2003). The parties dispute the applicability to this case of the Supreme Court's recent decision, Festo Corp v Shoketsu Kinzoku Kogyo Kabushiki Co, 535 US 722, 733 (2002). The court finds that it is unnecessary to determine whether the

presumption related to the scope of proven prosecution history estoppel applies to argument-based estoppel.

The court must also consider the all elements rule, which requires the court to determine whether a "finding of infringement under the doctrine of equivalents would entirely vitiate a particular claimed element." Lockheed Martin, 324 F3d at 1321; Warner-Jenkinson Co, 520 US at 39 n8 ("[I]f a theory of equivalence would entirely vitiate a particular claim element, partial or complete judgment should be rendered by the court, as there would be no further material issue for the jury to resolve.").

If the court finds, as a matter of law, that the patent holder's claim of equivalence is neither barred by the prosecution history nor by the all elements rule, then the factual question of equivalence may be considered. An accused device practices an element of the claim if it performs substantially the same function, in substantially the same way, to achieve substantially the same result or if the accused device contains only an insubstantial difference. Warner-Jenkinson Co, 520 US at 39-40.

B

FRCP 56(c) provides that judgment may be granted if the factual record in the case demonstrates that "there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law." A party seeking summary judgment bears the initial burden of identifying that there is no genuine issue as to a material fact. Celotex Corp v

Catrett, 477 US 317, 323 (1986). Because Ritek, as the moving party, will not have the burden of proof at trial, Ritek can prevail by identifying an absence of evidence to support SanDisk's case. Id. If Ritek meets this initial burden, SanDisk must then set forth "specific facts showing that there is a genuine issue for trial." Anderson v Liberty Lobby, Inc, 477 US 242, 250 (1986).

At the summary judgment stage, the court does not make credibility determinations or weigh conflicting evidence, but draws all inferences in the light most favorable to the non-moving party. T W Elec Service, Inc v Pac Elec Contractors Ass'n, 809 F2d 626, 630-31 (9th Cir 1987). The evidence presented must be admissible. FRCP 56(e). Conclusory or speculative language is insufficient to create a genuine issue of fact to defeat summary judgment. See Mitchel v General Elec Co, 689 F2d 877, 878 (9th Cir 1982).

In considering literal infringement at the summary judgment stage, "it must be shown that, on the correct claim construction, no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee." Netword, 242 F3d at 1353. The court takes special care in examining summary judgment under the doctrine of equivalents, because "[i]nfringement under the doctrine of equivalents requires an intensely factual inquiry." Toro Co v White Consol Ind, Inc, 266 F3d 1367, 1369-70 (Fed Cir 2001) (internal quotation omitted). In the end, however, the summary judgment standard remains the same for literal infringement or infringement under

the doctrine of equivalents. See Sage Prods v Devon Indus, Inc, 126 F3d 1420, 1423 (Fed Cir 1997) ("Although equivalence is a factual matter normally reserved for a factfinder, the trial court should grant summary judgment in any case where no reasonable factfinder could find equivalence.").

C

Ritek argues that it does not literally infringe because its products "have blocks that contain only overhead data portions." Ritek Mot (Doc # 208) at 7. Ritek further argues that these overhead-only blocks are "essential to any method of operating Ritek's accused products." Id at 8. The court notes that Ritek misstates the analysis that the court needs to undertake. The question is not whether Ritek's products require these overhead-only blocks, but whether Ritek's products practice each element of the '987 patent. An accused device may infringe even if it requires steps in addition to elements claimed by the patent. Smith & Nephew, Inc, 276 F3d at 1311. If Ritek's overhead-only blocks were used in an additional step, then the mere fact that they are necessary for operation of Ritek's products would not influence the court's analysis.

As noted above, claims 1 and 10 of the '987 patent contain the following limitations:

> An array of non-volatile floating gate memory cells contains a group of memory cells on one or more memory chips. Multiple chips in the same array are connected to a common interface and/or common logic and resistor

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> circuits. An array may contain components that are not memory cells, such as an interface.
>
> * * *
>
> Each non-volatile memory sector contained within an array of non-volatile floating gate memory cells must include at least one user data portion and one overhead portion. Memory sectors are not limited to only one user data portion and one overhead portion.

Supra.

SanDisk's arguments against summary judgment of literal non-infringement fail based on the above claim construction. SanDisk argues that the partitioning element of claims 1 and 10 only requires that all sectors that contain user data must be partitioned into user data and overhead portions. SanDisk Br (Doc # 271) at 7-9. SanDisk cites defective sectors as specific evidence of this interpretation. The court rejects SanDisk's contention because the court's claim construction requires all sectors within the memory array to be partitioned. SanDisk also argues that Ritek's products literally infringe because they contain some memory chips in which all the sectors are partitioned into user data and overhead portions. Id at 10. This argument fails because the court finds that the array described by claims 1 and 10 is an inter-chip array.

Ritek's products do not practice each element of claims 1 and 10 of the '987 patent, because they do not "partition[] the memory cells within the individual sectors into at least a user data portion and an overhead portion." '987 patent at 16:35-37; 17:42-44. Ritek's memory cards are limited to a single array of memory cells. Chiu Decl I (Doc # 284, Exh K) at 2. Within this array, not all of the blocks are partitioned

into user data and overhead portions. Id at 4-8; Chiu Decl II (Doc # 284, Exh J) at 3-6. Accordingly, the court finds that Ritek's products do not literally infringe the '987 patent.

D

SanDisk argues, in the alternative, that Ritek's products infringe under the doctrine of equivalents. As noted above, the court must first consider, as a question of law, whether the prosecution history estops SanDisk from this claim or whether SanDisk's claim would violate the all elements rule.

Prosecution history estoppel concerning partitioning in this case is based exclusively on arguments made by SanDisk to the patent examiner, rather than on amendments. The "clear and unmistakable" standard for argument-based estoppel is the same as the standard for prosecution disclaimer, discussed above. See Omega Engr, Inc v Raytek Corp, 334 F3d 1314, 1326 n1 (Fed Cir 2003). The court finds, in accordance with its claim construction above, that the prosecution history estops SanDisk from asserting that only some of the sectors contained within the array need to be partitioned into at least user data and overhead portions. SanDisk clearly and unmistakably argued to the patent examiner that each sector must be partitioned under claims 1 and 10.

The court also finds, alternatively, that an extension of the claims to allow some sectors within the array to be partitioned into only an overhead portion would entirely vitiate the claim limitation. In Sage Products, the Federal Circuit considered two patent holders who held patents covering disposal

devices for biomedical waste. Sage Prods, 126 F3d 1420. Each patent holder was suing the other for infringement. The court found that neither infringed the other's patent. In doing so, the court rejected the claims of each patent holder under the "entirely vitiate" standard of the all elements rule. The plaintiff claimed that "having two constrictions below the top of the container is the same, for purposes of infringement, as having one constriction above and one constriction below." Id at 1424. The court rejected this argument, finding that it would "remove entirely" the top of the container limitation of the claim. Similarly, the defendant claimed that a "permanently locking lid is equivalent * * * to an openable lid." Id at 1429. The court also rejected this argument, finding that allowing the argument would require the court to "remove an express functional requirement of the claim." Id.

In Moore, the Federal Circuit also applied the all elements rule. Moore USA, Inc v Standard Register Co, 229 F3d 1091 (Fed Cir 2000). In Moore, the accused device contained longitudinal strips of adhesive that extended approximately 48% along the length of the longitudinal margins in the device. The patent at issue in Moore contained a limitation that required longitudinal strips of adhesive to extend at least a majority of the length of the longitudinal margins of the device. Id at 1106. The Moore court rejected the patent holder's argument that finding the 2% difference between the accused device and the patent claim equivalent "would not vitiate the 'majority of the lengths' limitation." Id. Instead, the Moore court found that "it would defy logic to conclude that a majority–the very

antithesis of a majority–could be insubstantially different from a claim limitation requiring a majority." Id.

Here, SanDisk argues that finding Ritek's products to infringe under the doctrine of equivalents would not entirely vitiate the partitioning element, because Ritek's products contain only a small number of overhead-only blocks. SanDisk Br (Doc # 271) at 18:21-24 (arguing that the Ritek product is equivalent to the claim because the "vast majority of the sectors on Ritek's CompactFlash cards satisfy this 'partitioning'"); id at 19:26-20:13 (noting that less than 1% of the total number of the blocks in Ritek's products are overhead-only blocks). The court must reject this argument. As in Moore, the mere fact that a small percentage separates the claim from the accused device does not control. The court finds that the partitioning element requires each sector to be partitioned into at least user data and overhead portions. Changing this construction from "each" to "some" would entirely vitiate the limitation.

## VII

Accordingly, the court DENIES defendants' administrative request to strike SanDisk's February 22, 2002, claims construction statement (Doc # 245). The court GRANTS Ritek's motion for summary judgment of non-infringement (Doc # 208). The court DENIES the Memorex and Pretec joinder in Ritek's motion for summary judgment (Doc # 236). The clerk is directed to terminate all motions pending that relate to the SanDisk-Ritek action. See Docs ## 191, 195, 208, 216, 236, 245,

254, 260, 265, 274, 275, 278, 285 & 316. The court DIRECTS SanDisk and defendants Memorex and Pretec to attend a CMC at 9:00 am on November 6, 2003, or if this date is not convenient, the court DIRECTS the remaining parties to confer to determine an alternative date and contact the deputy clerk to set up a conference at a date convenient to their schedules.

IT IS SO ORDERED.

VAUGHN R WALKER
United States District Judge